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10/597,728	09/17/2007	Christopher Gordon Turner	054054/315213	5449

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EXAMINER	
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/597,728	TURNER ET AL.	
	Examiner	Art Unit	
	JAMES YANG	2612	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 December 2011*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

4)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

5)☒ Claim(s) *1-27,29-33 and 35-46* is/are pending in the application.

5a) Of the above claim(s) _____ is/are withdrawn from consideration.

6)☐ Claim(s) _____ is/are allowed.

7)☒ Claim(s) *1-27,29-33 and 35-46* is/are rejected.

8)☐ Claim(s) _____ is/are objected to.

9)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

10)☐ The specification is objected to by the Examiner.

11)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

12)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to applicant's amendment filed 12/28/2011.

Claims 1-27, 29-33, 35-46 are currently pending in this application.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

Claim 46 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification (see Paragraph [0023]) does not explicitly disclose how the logic circuitry of the method of claim 46 is able to control at least one of the data lines, but not control all of the data lines. Also, claim 46 appears to have a negative limitation. Any negative limitation or exclusionary proviso must have basis in the original disclosure. If alternative elements are positively recited in the specification, they may be explicitly excluded in the claims. See In re Johnson, 558 F.2d 1008, 1019, 194 USPQ 187, 196 (CCPA 1977) ("[the] specification, having described the whole, necessarily described the part remaining."). See also Ex parte Grasselli, 231 USPQ 393 (Bd. App. 1983), *aff 'd*

mem., 738 F.2d 453 (Fed. Cir. 1984). The mere absence of a positive recitation is not basis for an exclusion.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

1. Claims 1-6, 8-15, 17-22, 24-27, 29-33, 35-40, and 42-44 are rejected under 35 U.S.C. 102(b) as being anticipated by Van Eeden (U.S. 6,154,136).

Claim 1, Van Eeden teaches:

A method of identifying a plurality of transponders in an interrogation process (Van Eeden, Col. 3, Lines 53-65**) comprising:**

transmitting an interrogation signal to the transponders (Van Eeden, Col. 3, Lines 53-54**);**

receiving a response signal from each transponder (Van Eeden, Col. 3, Lines 61-65**) at a time within a respective waiting period (**Van Eeden, Col. 4, Lines 16-19, The random inter-transmission intervals are the waiting periods, because the transponder must wait for each random inter-transmission interval to expire before re-transmitting (see Van Eeden, Col. 4, Lines 33-39).**) the**

maximum duration of which can be adjusted (Van Eeden, Col. 4, Lines 40-49**);**

creating a plurality of data line signals together defining a random number (Van Eeden, Fig. 2, Col. 4, Lines 21-39, The random inter-transmission interval generation means 34 includes multiple components connected by a circuit, or data lines, that create and define a random inter-transmission interval, which is a random number.**);**

feeding said data line signals to a counter on respective ones of a plurality of data lines for determining the waiting period (Van Eeden, Col. 4, Lines 30-39, The comparator determines when a counter value equals a random number in order to determine whether a signal burst is enabled or whether the transponder should continue to wait. Therefore, the comparator may be interpreted as a counter, since the comparator performs the same function. As can be seen in the drawing, the comparator receives multiple signals from multiple sources, i.e. respective ones of a plurality of data lines.**); and**

providing *at least one of* the data lines with logic circuitry wherein the logic circuitry is configured to control the at least one of the data lines to block or permit the respective data line signal to be received by the counter (Van Eeden, Col. 4, Lines 21-39, The random inter-transmission interval generation means is logic circuitry that permits data to be sent to the comparator.**) thereby adjusting a total number of data line signals reaching the input of the counter to control the maximum length of the waiting period (**Van Eeden, Col. 4, Lines 50-67, The maximum value of N_{max} is

determined by a combination of signals from counter 44, counter 66, and the number of bits in the random number.**).**

Claim 2, Van Eeden teaches:

A method of identifying a plurality of transponders in an interrogation process (Van Eeden, Col. 3, Lines 53-65**) comprising:**

transmitting an interrogation signal to the transponders (Van Eeden, Col. 3, Lines 53-54**);**

receiving a response signal from each transponder (Van Eeden, Col. 3, Lines 61-65**) during a respective waiting period (**Van Eeden, Col. 4, Lines 16-19, The random inter-transmission intervals are the waiting periods, because the transponder must wait for each random inter-transmission interval to expire before re-transmitting (see Van Eeden, Col. 4, Lines 33-39).**) a maximum duration of the waiting period being adjustable (**Van Eeden, Col. 4, Lines 40-49**); and**

for each transponder:

transmitting output signals on respective ones of a plurality of data lines from a random number generator of the transponder to respective inputs of a counter of the transponder for determining the waiting period (Van Eeden, Col. 4, Lines 30-39, The comparator determines when a counter value equals a random number in order to determine whether a signal burst is enabled or whether the transponder should continue to wait. Therefore, the comparator may be interpreted as a counter, since the comparator performs the

same function. As can be seen in the drawing, the comparator receives multiple signals from multiple sources, i.e. respective ones of a plurality of data lines.**), at least one of the output signals from the random number generator being fed via logic circuitry to a respective input of the counter (**Van Eeden, Col. 4, Lines 30-39**); and**

controlling the logic circuitry to adjust the maximum length of the waiting period (Van Eeden, Col. 4, Lines 50-67, The maximum value of N_{max} is determined by a combination of signals from counter 44, counter 66, and the number of bits in the random number.**).**

Claim 3, Van Eeden further teaches:

The logic circuitry comprises one or more logic gates (Van Eeden, Fig. 2: 40, Col. 4, Lines 35-39, The comparator 40 receives up to three inputs, and generates a single output based on a comparison of the inputs. Thus, the comparator is a logic gate.**), the number of logic gates being less than the number of data lines (**Van Eeden, Fig. 2: 40, Col. 4, Lines 35-39, Each of the data inputs to the comparator 40 may be interpreted as a data line, thus there are less logic gates than data lines.**).**

Claim 4, Van Eeden further teaches:

The waiting period consists of a plurality of smaller time intervals or time slots together defining a Round Size representative of that waiting period (Van Eeden, Fig. 3: 22.1-22.4, Col. 4, Line 1, Each of the inter-

transmission values have a length or Round Size, and as can be seen in the figure, there are a plurality of smaller time intervals defining a waiting period.**).**

Claim 5, Van Eeden further teaches:

There is a minimum Round Size and at least one larger Round Size (Van Eeden, Fig. 3: 22.1-22.4, Col. 4, Lines 40-49, The term round size is generally interpreted as the size of the minimum interval value.**), the or each larger Round Size consisting of a combination of minimum Round Sizes (**Van Eeden, Col. 4, Lines 40-67, Since the maximum inter-transmission interval or round size, N_{max}, is increasing, and the N_{max} is larger than the minimum inter-transmission interval, the maximum inter-transmission interval is a combination of the minimum inter-transmission interval. For example, if N_{max} = 15 (like the example in Van Eeden), and the minimum is 1, then the N_{max} is a combination or multiple of 15 minimum values.**), whereby controlling the logic circuitry determines the number of minimum Round Sizes to be combined to define the desired larger Round Size to be used (**Van Eeden, Col. 4, Lines 40-67**).**

Claim 6, Van Eeden further teaches:

By controlling the logic circuitry the maximum duration of the waiting period is increased or decreased by multiples of 2 or 0.5 respectively (Van Eeden, Col. 4, Lines 50-67**).**

Claim 8, Van Eeden further teaches:

The step of clocking the random number generator and/or clocking the counter by means of a clock oscillator of the transponder (Van Eeden, Col. 4, Lines 30-39, The term “clocking” the counter is resetting the counter by means of a clock in the transponder. It is noted that by resetting counter 38, the comparator 40 is effectively reset too since the comparator requires an input from counter 38 in order to make a comparison.**).**

Claim 9, Van Eeden further teaches:

Causing the transponder to transmit an output signal from its transmitter when the counter has been counted to its terminal count (Van Eeden, Col. 4, Lines 34-39**), whereupon the counter loads a fresh or new number from the random number generator for the next count (**Van Eeden, Col. 4, Lines 30-35**).**

Claim 10, Van Eeden further teaches:

Determining the maximum possible waiting time or maximum possible number of slots over which to randomize transmissions of the output signal from the transmitter by the length of the counter (Van Eeden, Col. 4, Lines 50-67**), the data lines between the random number generator and the counter being gated in order "fold" the counter such that the effective counter length may be modified in multiples of two (**Van Eeden, Col. 4, Lines 50-67, The preferred modification of the maximum value is by multiples of 2.**).**

Claim 11, Van Eeden further teaches:

Deriving the random number by taking a snapshot of the transponder clock, or by a hash value received from the interrogator in a command (Van Eeden, Col. 4, Lines 30-39, The counter 38 is incremented by each pulse of clock 48, thus a snapshot is taken. Thus, when the counter 38 equals the random number generated by random number generator 36, i.e. deriving the random number, the transponder transmits a pulse.**).**

Claim 12, Van Eeden further teaches:

Using either an up or a down counter whereby the terminal value of the counter is reached with the clocking signal causing the counter to either increment or decrement as required (Van Eeden, Col. 4, Lines 30-39**).**

Claim 13, Van Eeden further teaches:

The output response signal contains identity or field data of a tag or transponder (Van Eeden, Col. 3, Lines 54-60**).**

Claim 14, Van Eeden further teaches:

Transponders not already included in an active population under interrogation are arranged to enter said active population (Van Eeden, Col. 3, Lines 53-60, Tags being read are not in an active population and are arranged to enter the population.**), whereupon said transponders entering the active**

population receive a signal from the interrogator to adjust the maximum length of their waiting period (Van Eeden, Col. 4, Lines 15-29 and Lines 40-49, Upon interrogation, the tags adjust its maximum inter-transmission interval. Thus, the energizing signal 16 causes the transponders to adjust the maximum length of their waiting periods.**).**

Claim 15, Van Eeden further teaches:

The adjusted maximum length of the waiting period of the transponders, after arriving into an already existing active population under interrogation, is chosen to ensure transmissions from said transponders occur at an appropriate stage in the arbitration to facilitate reading of those transponders entering the active population (Van Eeden, Figs. 3-4, Col. 3, Lines 66-66 through Col. 4, Lines 1-14, and Col. 4, Lines 40-49, The random inter-transmission intervals are created such that each transponder in the population responds to an interrogation signal at different times.**).**

Claim 17, Van Eeden teaches:

A transponder (Van Eeden, Col. 3, Lines 61-65 and Col. 4, Lines 16-19**), comprising:**

means for deriving a random number within the transponder (Van Eeden, Fig. 2, Col. 4, Lines 21-39, The random inter-transmission interval generation means 34 includes multiple components connected by a circuit, or

data lines, that create and define a random inter-transmission interval, which is a random number.**); and**

means for delivering the random number by way of binary output signals along respective ones of a plurality of data lines to a counter (Van Eeden, Col. 4, Lines 30-39, The comparator determines when a counter value equals a random number in order to determine whether a signal burst is enabled or whether the transponder should continue to wait. Therefore, the comparator may be interpreted as a counter, since the comparator performs the same function. As can be seen in the drawing, the comparator receives multiple signals from multiple sources, i.e. respective ones of a plurality of data lines.**), wherein at least one of the data lines is connected to the counter via logic circuitry (**Van Eeden, Col. 4, Lines 21-39, The random inter-transmission interval generation means is logic circuitry that permits data to be sent to the comparator.**), wherein control of the logic circuitry can block or permit the data line signal to the counter (**Van Eeden, Col. 4, Lines 21-39, The random inter-transmission interval generation means is logic circuitry that permits data to be sent to the comparator.**) thereby adjusting the total number of data line signals reaching the input of the counter to control the maximum length of the waiting period (**Van Eeden, Col. 4, Lines 50-67, The maximum value of N_{max} is determined by a combination of signals from counter 44, counter 66, and the number of bits in the random number.**).**

Claim 18, Van Eeden teaches:

A transponder (Van Eeden, Col. 3, Lines 61-65 and Col. 4, Lines 16-19**), the transponder comprising:**

a random number generator (Van Eeden, Fig. 2, Col. 4, Lines 21-39, The random inter-transmission interval generation means 34 includes multiple components connected by a circuit, or data lines, that create and define a random inter-transmission interval, which is a random number.**) configured to generate binary output signals on respective ones of a plurality of data lines which are fed to the inputs of a counter for determining the waiting period (**Van Eeden, Col. 4, Lines 30-39, The comparator determines when a counter value equals a random number in order to determine whether a signal burst is enabled or whether the transponder should continue to wait. Therefore, the comparator may be interpreted as a counter, since the comparator performs the same function. As can be seen in the drawing, the comparator receives multiple signals from multiple sources, i.e. respective ones of a plurality of data lines.**), wherein at least one of the output signals from the random number generator is fed via logic circuitry to a respective input of the counter (**Van Eeden, Col. 4, Lines 21-39, The random inter-transmission interval generation means is logic circuitry that permits data to be sent to the comparator.**) whereby control of the logic circuitry adjusts the maximum length of the waiting period (**Van Eeden, Col. 4, Lines 50-67, The maximum value of N_{max} is determined by a combination of signals from counter 44, counter 66, and the number of bits in the random number.**).**

Claim 19, Van Eeden further teaches:

The logic circuitry comprises one or more logic gates (Van Eeden, Fig. 2: 40, Col. 4, Lines 35-39, The comparator 40 receives up to three inputs, and generates a single output based on a comparison of the inputs. Thus, the comparator is a logic gate.**), the number of logic gates being less than the number of data lines for the binary output signals (**Van Eeden, Fig. 2: 40, Col. 4, Lines 35-39, Each of the data inputs to the comparator 40 may be interpreted as a data line, thus there are less logic gates than data lines. Data being transferred includes bits (see Van Eeden, Col. 2, Lines 63-67 through Col. 3, Lines 1-4).**).**

Claim 20, Van Eeden further teaches:

The waiting period consists of a plurality of smaller time intervals or time slots together defining a Round Size representative of that waiting period (Van Eeden, Fig. 3: 22.1-22.4, Col. 4, Line 1, Each of the inter-transmission values have a length or Round Size, and as can be seen in the figure, there are a plurality of smaller time intervals defining a waiting period.**).**

Claim 21, Van Eeden further teaches:

There is a minimum Round Size and at least one larger Round Size (Van Eeden, Fig. 3: 22.1-22.4, Col. 4, Lines 40-49, The term round size is generally interpreted as the size of the minimum interval value.**), the or each larger Round Size consisting of a combination of minimum Round Sizes**

(Van Eeden, Col. 4, Lines 40-67, Since the maximum inter-transmission interval or round size, N_{max}, is increasing, and the N_{max} is larger than the minimum inter-transmission interval, the maximum inter-transmission interval is a combination of the minimum inter-transmission interval. For example, if N_{max} = 15 (like the example in Van Eeden), and the minimum is 1, then the N_{max} is a combination or multiple of 15 minimum values.**), whereby controlling the logic circuitry determines the number of minimum Round Sizes to be combined to define the desired larger Round Size to be used (**Van Eeden, Col. 4, Lines 40-67**).**

Claim 22, Van Eeden further teaches:

The logic circuitry is arranged to enable the maximum duration of the waiting period to be increased or decreased by multiples of 2 or 0.5 respectively (Van Eeden, Col. 4, Lines 50-67**).**

Claim 24, Van Eeden further teaches:

The transponder dynamically alters the maximum waiting time in response to an instruction from an interrogator (Van Eeden, Col. 4, Lines 40-67, The transponder performs the maximum value based upon the number of transmission bursts required, each of the transmission bursts are in response to an interrogation signal from the reader (see Van Eeden, Col. 3, Lines 53-60).**).**

Claim 25, Van Eeden further teaches:

The transponder is adapted to detect either heavy signal congestion or large quiet signal periods and alter the maximum waiting time accordingly (Van Eeden, Col. 4, Lines 40-67, The transponder can determine the maximum inter-transmission interval value based upon the number in the incremental counter. The larger the value of the counter, the larger possible inter-transmission intervals, thus the transponder can detect this larger possible value, i.e. large quiet signal periods, based upon the incremental counter, and continues to increase this value. It is noted that the examiner believes the applicant intends on claiming that the transponder can detect quiet periods between other transponders, but the claims allow for multiple interpretations.**).**

Claim 26, Van Eeden further teaches:

The transponder is adapted to alter the maximum waiting time in response to an instruction from the interrogator or in response to external conditions present during the interrogation (Van Eeden, Col. 4, Lines 40-67, The transponder performs the maximum value based upon the number of transmission bursts required, each of the transmission bursts are in response to an interrogation signal from the reader (see Van Eeden, Col. 3, Lines 53-60).**).**

Claim 27, Van Eeden teaches:

A transponder comprising:

a receiver for receiving an interrogation signal from an interrogator (Van Eeden, Col. 3, Lines 53-60, The transponder receives the signal in order to generate a response signal.**);**

a transmitter for transmitting a response signal after receipt of the interrogation signal (Van Eeden, Col. 3, Lines 53-60, The response signals are transmitted by a transponder transmitter (see Van Eeden, Fig. 2: 30, Col. 4, Lines 16-19).**);**

means for generating the response signal during a waiting period (Van Eeden, Col. 4, Lines 15-20**); and**

a random number generator (Van Eeden, Fig. 2, Col. 4, Lines 21-39, The random inter-transmission interval generation means 34 includes multiple components connected by a circuit, or data lines, that create and define a random inter-transmission interval, which is a random number.**) for generating binary output signals which are fed via respective ones of a plurality of data lines to inputs of a counter for determining the waiting period (**Van Eeden, Col. 4, Lines 30-39, The comparator determines when a counter value equals a random number in order to determine whether a signal burst is enabled or whether the transponder should continue to wait. Therefore, the comparator may be interpreted as a counter, since the comparator performs the same function. As can be seen in the drawing, the comparator receives multiple signals from multiple sources, i.e. respective ones of a plurality of data lines.**), wherein at least one of the output signals from the random number generator is fed via a data line having logic circuitry to a respective input of**

the counter (Van Eeden, Col. 4, Lines 21-39, The random inter-transmission interval generation means is logic circuitry that permits data to be sent to the comparator.**), wherein control of the logic circuitry adjusts the maximum length of the waiting period during interrogation by the interrogator (**Van Eeden, Col. 4, Lines 50-67, The maximum value of N_{max} is determined by a combination of signals from counter 44, counter 66, and the number of bits in the random number.**).**

Claim 29, Van Eeden further teaches:

The random number is derived by taking a snapshot of the transponder clock, or by a hash value received from a command from an interrogator (Van Eeden, Col. 4, Lines 30-39, The counter 38 is incremented by each pulse of clock 48, thus a snapshot is taken. Thus, when the counter 38 equals the random number generated by random number generator 36, i.e. deriving the random number, the transponder transmits a pulse.**).**

Claim 30, Van Eeden further teaches:

The counter is an up or a down counter whereby the terminal value of the counter is reached with the clocking signal causing the counter to either increment or decrement as required (Van Eeden, Col. 4, Lines 30-39**).**

Claim 31, Van Eeden further teaches:

A memory for storing an identity or data field (Van Eeden, Fig. 2: 32, Col. 4, Lines 19-20**) and a modulator for transmitting the identity or data as a message in the output response signal (**Van Eeden, Col. 4, Lines 15-20, The transponder transmits its signal using a transmitter stage 30, which is interpreted as a modulator.**).**

Claim 32, Van Eeden teaches:

An identification system comprising:

an interrogator and a plurality of transponders (Van Eeden, Fig. 1, Col. 3, Lines 49-52**),**

the interrogator including a transmitter for transmitting an interrogation signal to the transponders (Van Eeden, Col. 3, Lines 53-54, The reader has a transmitter in order to transmit the energizing signal 16.**),**

each transponder including:

a receiver for receiving the interrogation signal (Van Eeden, Col. 3, Lines 53-60, Each transponder has a receiver for receiving the energizing signal 16.**),**

a transmitter for transmitting a response signal after receipt of the interrogation signal (Van Eeden, Col. 3, Lines 54-60 and Col. 4, Lines 15-20**) and**

means for generating the response signal during a waiting period (Van Eeden, Col. 4, Lines 15-20**),**

each transponder having means for altering a maximum length of the waiting period during interrogation of the transponders by the interrogator (Van Eeden, Col. 4, Lines 40-67**),**

the transponder further including a random number generator (Van Eeden, Fig. 2, Col. 4, Lines 21-39, The random inter-transmission interval generation means 34 includes multiple components connected by a circuit, or data lines, that create and define a random inter-transmission interval, which is a random number.**) for generating binary output signals which are fed via respective ones of a plurality of data lines to the inputs of a counter for determining the waiting period (**Van Eeden, Col. 4, Lines 30-39, The comparator determines when a counter value equals a random number in order to determine whether a signal burst is enabled or whether the transponder should continue to wait. Therefore, the comparator may be interpreted as a counter, since the comparator performs the same function. As can be seen in the drawing, the comparator receives multiple signals from multiple sources, i.e. respective ones of a plurality of data lines.**),**

wherein at least one of the output signals from the random number generator is fed via a data line having logic circuitry to a respective input of the counter (Van Eeden, Col. 4, Lines 21-39, The random inter-transmission interval generation means is logic circuitry that permits data to be sent to the comparator.**) whereby control of the logic circuitry adjusts the maximum length of the waiting period (**Van Eeden, Col. 4, Lines 50-67, The maximum

value of N_{max} is determined by a combination of signals from counter 44, counter 66, and the number of bits in the random number.**).**

Claim 33, Van Eeden teaches:

An identification system comprising:

an interrogator and a plurality of transponders (Van Eeden, Fig. 1, Col. 3, Lines 49-52**),**

the interrogator including a transmitter for transmitting an interrogation signal to the transponders (Van Eeden, Col. 3, Lines 53-54, The reader has a transmitter in order to transmit the energizing signal 16.**),**

each transponder including:

a receiver for receiving the interrogation signal (Van Eeden, Col. 3, Lines 53-60, Each transponder has a receiver for receiving the energizing signal 16.**),**

a transmitter for transmitting a response signal after receipt of the interrogation signal (Van Eeden, Col. 3, Lines 54-60 and Col. 4, Lines 15-20**),**

means for generating the response signal during a waiting period (Van Eeden, Col. 4, Lines 15-20**),**

means for altering the maximum length of the waiting period during interrogation of the transponders by the interrogator (Van Eeden, Col. 4, Lines 40-67**), the transponders having means for deriving a random number within the transponder (**Van Eeden, Fig. 2, Col. 4, Lines 21-39, The random inter-transmission interval generation means 34 includes multiple components

connected by a circuit, or data lines, that create and define a random inter-transmission interval, which is a random number.**) and delivering the random number by way of binary output signals along respective ones of a plurality of data lines to a counter (**Van Eeden, Col. 4, Lines 30-39, The comparator determines when a counter value equals a random number in order to determine whether a signal burst is enabled or whether the transponder should continue to wait. Therefore, the comparator may be interpreted as a counter, since the comparator performs the same function. As can be seen in the drawing, the comparator receives multiple signals from multiple sources, i.e. respective ones of a plurality of data lines.**),**

wherein at least one of the data lines is connected to the counter via logic circuitry whereby control of the logic circuitry can block or permit the data line signal to the counter (Van Eeden, Col. 4, Lines 21-39, The random inter-transmission interval generation means is logic circuitry that permits data to be sent to the comparator.**) thereby adjusting the total number of data line signals reaching the input of the counter to control the maximum length of the waiting period (**Van Eeden, Col. 4, Lines 50-67, The maximum value of N_{max} is determined by a combination of signals from counter 44, counter 66, and the number of bits in the random number.**).**

Claim 35, Van Eeden teaches:

An integrated circuit for use in a transponder of an RFID interrogation system (Van Eeden, Fig. 2**), the integrated circuit comprising:**

a receiver for receiving an interrogation signal (Van Eeden, Col. 3, Lines 53-60, Each transponder has a receiver for receiving the energizing signal 16.**);**

a transmitter for transmitting a response signal after receipt of the interrogation signal (Van Eeden, Col. 3, Lines 54-60 and Col. 4, Lines 15-20**);**

means for generating the response signal during a waiting period (Van Eeden, Col. 4, Lines 15-20**);**

control means for altering the maximum length of the waiting period (Van Eeden, Col. 4, Lines 40-67**);**

means for deriving a random number within the integrated circuit (Van Eeden, Fig. 2, Col. 4, Lines 21-39, The random inter-transmission interval generation means 34 includes multiple components connected by a circuit, or data lines, that create and define a random inter-transmission interval, which is a random number.**) and delivering the random number by way of binary output signals along respective ones of a plurality of data lines to a counter (**Van Eeden, Col. 4, Lines 30-39, The comparator determines when a counter value equals a random number in order to determine whether a signal burst is enabled or whether the transponder should continue to wait. Therefore, the comparator may be interpreted as a counter, since the comparator performs the same function. As can be seen in the drawing, the comparator receives multiple signals from multiple sources, i.e. respective ones of a plurality of data lines.**) and wherein at least one of the data lines is connected to the counter via logic circuitry control of which can block or permit the data line signal to**

the counter (Van Eeden, Col. 4, Lines 21-39, The random inter-transmission interval generation means is logic circuitry that permits data to be sent to the comparator.**) thereby adjusting the total number of data line signals reaching the input of the counter to control the maximum length of the waiting period (**Van Eeden, Col. 4, Lines 50-67, The maximum value of N_{max} is determined by a combination of signals from counter 44, counter 66, and the number of bits in the random number.**).**

Claim 36, Van Eeden teaches:

An integrated circuit for use in a transponder (Van Eeden, Fig. 2**) comprising:**

a receiver for receiving an interrogation signal (Van Eeden, Col. 3, Lines 53-60, Each transponder has a receiver for receiving the energizing signal 16.**);**

a transmitter for transmitting a response signal after receipt of the interrogation signal (Van Eeden, Col. 3, Lines 54-60 and Col. 4, Lines 15-20**);**

means for generating the response signal during a waiting period (Van Eeden, Col. 4, Lines 15-20**);**

control means for altering the maximum length of the waiting period during interrogation of the transponder by the interrogator (Van Eeden, Col. 4, Lines 40-67**);**

a random number generator (Van Eeden, Fig. 2, Col. 4, Lines 21-39, The random inter-transmission interval generation means 34 includes multiple

components connected by a circuit, or data lines, that create and define a random inter-transmission interval, which is a random number.**) for generating binary output signals which are fed via respective ones of a plurality of data lines to the inputs of a counter for determining the waiting period (**Van Eeden, Col. 4, Lines 30-39, The comparator determines when a counter value equals a random number in order to determine whether a signal burst is enabled or whether the transponder should continue to wait. Therefore, the comparator may be interpreted as a counter, since the comparator performs the same function. As can be seen in the drawing, the comparator receives multiple signals from multiple sources, i.e. respective ones of a plurality of data lines.**);**

a logic circuitry, wherein at least one of the output signals from the random number generator is fed via the logic circuitry to a respective input of the counter (Van Eeden, Col. 4, Lines 21-39, The random inter-transmission interval generation means is logic circuitry that permits data to be sent to the comparator.**), control of the logic circuitry thereby providing means for adjusting the maximum length of the waiting period (**Van Eeden, Col. 4, Lines 50-67, The maximum value of N_{max} is determined by a combination of signals from counter 44, counter 66, and the number of bits in the random number.**).**

Claim 37, Van Eeden further teaches:

The logic circuitry comprises one or more logic gates (Van Eeden, Fig. 2: 40, Col. 4, Lines 35-39, The comparator 40 receives up to three inputs,

and generates a single output based on a comparison of the inputs. Thus, the comparator is a logic gate.**), the number of logic gates being less than the number of data lines for the binary output signals to the counter (**Van Eeden, Fig. 2: 40, Col. 4, Lines 35-39, Each of the data inputs to the comparator 40 may be interpreted as a data line, thus there are less logic gates than data lines. Data being transferred includes bits (see Van Eeden, Col. 2, Lines 63-67 through Col. 3, Lines 1-4).**).**

Claim 38, Van Eeden further teaches:

The waiting period consists of a plurality of smaller time intervals or time slots together defining a Round Size representative of that waiting period (Van Eeden, Fig. 3: 22.1-22.4, Col. 4, Line 1, Each of the inter-transmission values have a length or Round Size, and as can be seen in the figure, there are a plurality of smaller time intervals defining a waiting period.**).**

Claim 39, Van Eeden further teaches:

There is a minimum Round Size and at least one larger Round Size (Van Eeden, Fig. 3: 22.1-22.4, Col. 4, Lines 40-49, The term round size is generally interpreted as the size of the minimum interval value.**), the or each larger Round Size consisting of a combination of minimum Round Sizes (**Van Eeden, Col. 4, Lines 40-67, Since the maximum inter-transmission interval or round size, N_{max}, is increasing, and the N_{max} is larger than the minimum inter-transmission interval, the maximum inter-transmission interval is a combination of

the minimum inter-transmission interval. For example, if N_{max} = 15 (like the example in Van Eeden), and the minimum is 1, then the N_{max} is a combination or multiple of 15 minimum values.**), whereby controlling the logic circuitry determines the number of minimum Round Sizes to be combined to define the desired larger Round Size to be used (**Van Eeden, Col. 4, Lines 40-67**).**

Claim 40, Van Eeden further teaches:

The logic circuitry is arranged to enable the maximum duration of the waiting period to be increased or decreased by multiples of 2 or 0.5 respectively (Van Eeden, Col. 4, Lines 50-67**).**

Claim 42, Van Eeden further teaches:

The random number is derived by taking a snapshot of the transponder clock, or by a hash value received from a command from an interrogator (Van Eeden, Col. 4, Lines 30-39, The counter 38 is incremented by each pulse of clock 48, thus a snapshot is taken. Thus, when the counter 38 equals the random number generated by random number generator 36, i.e. deriving the random number, the transponder transmits a pulse.**).**

Claim 43, Van Eeden further teaches:

The counter is an up or a down counter whereby the terminal value of the counter is reached with the clocking signal causing the counter to either increment or decrement as required (Van Eeden, Col. 4, Lines 30-39**).**

Claim 44, Van Eeden further teaches:

A memory for storing an identity or data field (Van Eeden, Fig. 2: 32, Col. 4, Lines 19-20**) and a modulator for transmitting the data in the output response signal (**Van Eeden, Col. 4, Lines 15-20, The transponder transmits its signal using a transmitter stage 30, which is interpreted as a modulator.**).**

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 7, 23, 41, and 46 are rejected under 35 U.S.C. 103(a) as being unpatentable over Van Eeden (U.S. 6,154,136).

Claim 7, Van Eeden further teaches:

By controlling the logic circuitry the desired Round Size is selected by increasing or decreasing the number of bits to be compared **(**Van Eeden, Col. 4, Lines 40-67, The value of N_{max} is increased by a factor of 2 which is then raised to the power of N.**).**

Van Eeden does not *explicitly* teach:

Increasing or decreasing the number of minimum Round Sizes to be combined, wherein available different Round Sizes are related to one another by factors or multiples of 2 or 0.5.

However, it would have been obvious to one of ordinary skill in the art at the time of the invention to choose a minimum value that is a whole number, because it is well-known in the art to use whole numbers to calculate binary numbers (see the example in Van Eeden, Col. 4, Lines 50-67), in order to establish a definitive range of inter-transmission intervals. Furthermore, it would have been obvious to one of ordinary skill in the art to choose the minimum Round Size value to be something small, such as 1, so that the range of numbers between the minimum Round Size value versus the maximum Round Size value would be the greatest, in order to increase the likelihood that different intervals be chosen. Thus, since the minimum Round Sizes to be combined defines the maximum Round Size, using a value such as 1 for the minimum Round Size causes the maximum Round Size to be a combination of the minimum round size by a multiple of 2 or 0.5. Since the claims only require the modifying of the minimum Round Sizes to be combined, instead of the minimum Round Size itself, the increasing of N_{max} in Van Eeden establishes that the value of N_{max} is greater than the minimum number.

Claims 23 and 41, Van Eeden teaches:

The logic circuitry is arranged to enable the desired Round Size to be selected by increasing or decreasing the number of bits to be compared **(**Van

Eeden, Col. 4, Lines 40-67, The value of N_{max} is increased by a factor of 2 which is then raised to the power of N.**).**

Van Eeden does not *explicitly* teach:

Increasing or decreasing the number of minimum Round Sizes to be combined, wherein available different Round Sizes are related to one another by factors or multiples of 2 or 0.5.

However, it would have been obvious to one of ordinary skill in the art at the time of the invention to choose a minimum value that is a whole number, because it is well-known in the art to use whole numbers to calculate binary numbers (see the example in Van Eeden, Col. 4, Lines 50-67), in order to establish a definitive range of inter-transmission intervals. Furthermore, it would have been obvious to one of ordinary skill in the art to choose the minimum Round Size value to be something small, such as 1, so that the range of numbers between the minimum Round Size value versus the maximum Round Size value would be the greatest, in order to increase the likelihood that different intervals be chosen. Thus, since the minimum Round Sizes to be combined defines the maximum Round Size, using a value such as 1 for the minimum Round Size causes the maximum Round Size to be a combination of the minimum round size by a multiple of 2 or 0.5. Since the claims only require the modifying of the minimum Round Sizes to be combined, instead of the minimum Round Size itself, the increasing of N_{max} in Van Eeden establishes that the value of N_{max} is greater than the minimum number.

Claim 46, Van Eeden teaches:

Providing the at least one logic circuitry includes providing the at least one logic circuitry to control the at least one of the data lines (Van Eeden, Col. 4, Lines 21-39, The random inter-transmission interval generation means is logic circuitry that permits data to be sent to the comparator.**),**

Van Eeden does not explicitly teach:

Providing the at least one logic circuitry not to control all of the data lines.

However, it would have been obvious to one of ordinary skill in the art at the time of the invention to eliminate the element of controlling specific data lines and it's function. Such a modification would not render the system and method inoperable for its intended function. See MPEP § 2144.04.

3. Claim 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Van Eeden (U.S. 6,154,136) in view of Ghaffari (U.S. 6,662,068).

Claim 16, Van Eeden teaches:

The transponders are associated with articles (Van Eeden, Col. 3, Lines 61-65)**.**

Van Eeden does not teach:

The transponders are moving relative to the interrogator.

Ghaffari teaches:

The transponders are moving relative to the interrogator (Ghaffari, Col. 12, Lines 37-46**).**

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the identification system in Van Eeden by integrating the teaching of moving articles as taught by Ghaffari.

The motivation would be to create an efficient tracking system of articles (see Ghaffari, Col. 12, Lines 37-46). It is also noted that it would have been obvious to modify the identification system in Van Eeden such that the system in the Van Eeden reference does not continuously read the same group of tags every time the interrogator is activated.

4. Claim 45 is rejected under 35 U.S.C. 103(a) as being unpatentable over Van Eeden (U.S. 6,154,136) in view of Ertin et al. (U.S. 2004/0198222).

Claim 45, Van Eeden teaches:

A reader for identifying a plurality of transponders (Van Eeden, Fig. 1, Col. 3, Lines 49-52**), the reader comprising:**

a transmitter for transmitting a reader signal to the transponders (Van Eeden, Col. 3, Lines 53-54, The reader has a transmitter in order to transmit the energizing signal 16.**);**

a receiver for receiving response signals from each transponder (Van Eeden, Col. 3, Lines 61-65, The reader has a receiver in order to receive the response signals from the transponders.**) at a time within a respective waiting**

period (Van Eeden, Col. 4, Lines 16-19, The random inter-transmission intervals are the waiting periods, because the transponder must wait for each random inter-transmission interval to expire before re-transmitting (see Van Eeden, Col. 4, Lines 33-39).**) the maximum duration of which can be adjusted (**Van Eeden, Col. 4, Lines 40-49**); and**

a processor for identifying a transponder from data in the response signal (Van Eeden, Col. 3, Lines 61-65, The reader has a device or component for identifying the transponders.**),**

wherein the reader comprises control means for controlling the reader signal (Van Eeden, Col. 3, Lines 53-60**) to control logic circuitry configured to control at least one of a plurality of binary output signals that are fed via respective ones of a plurality of data lines (**Van Eeden, Col. 4, Lines 30-39, The comparator determines when a counter value equals a random number in order to determine whether a signal burst is enabled or whether the transponder should continue to wait. Therefore, the comparator may be interpreted as a counter, since the comparator performs the same function. As can be seen in the drawing, the comparator receives multiple signals from multiple sources, i.e. respective ones of a plurality of data lines. The transponder performs these functions in response to an interrogation signal from the reader.**) connected to a counter in the transponder to adjust the maximum length of the waiting period (**Van Eeden, Col. 4, Lines 40-67**).**

Van Eeden does not teach:

The reader comprises detection means for detecting the number of collisions between response signals received at the receiver.

Ertin teaches:

The reader comprises detection means for detecting the number of collisions between response signals received at the receiver (Ertin, Paragraph [0037]**).**

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to modify the identification system in Van Eeden by integrating the teaching of detecting the number of collisions as taught by Ertin. The motivation would be to ensure all tags in a given area are read successfully by repeating a reader signal in case a collision is detected (see Ertin, Paragraph [0041]).

Response to Arguments

Applicant's arguments filed 12/28/2011have been fully considered but they are not persuasive.

In response to applicant's argument on Pages 15-16 that the Van Eden reference fails to teach each and every limitation, the examiner respectfully disagrees. Firstly, the claims recite that the logic circuitry is configured to block or permit the respective data line signal. Thus, if the system in Van Eeden permits signals on the data lines, then the reference reads on the claims, as either blocking or permitting is required, not both. Second, as can be seen in Fig. 2, the counter, i.e. comparator 40 and explained in the rejection above, receives

signals from a random number generator, a counter, and an interval counter. Thus, plurality of signals are generated and fed into the counter, wherein the arrows represent data lines (see also Van Eeden, Col. 4, Lines 30-49).

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES YANG whose telephone number is (571)270-5170. The examiner can normally be reached on M-F 8:30-5 EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Brian Zimmerman can be reached on 571-272-3059. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/J. Y./
Examiner, Art Unit 2612

/Brian A Zimmerman/
Supervisory Patent Examiner, Art Unit 2612